WHAT IS CLAIMED IS:

1. A method of testing a circuit under design having a plurality of functional elements and having a plurality of clock environments, at least one signal passing from one clock environment to another in said circuit, said method comprising the steps of:

modelling at least one of the functional elements to have an unknown state as an output for a predetermined time after a timing event of a clock signal;

simulating said circuit; and

determining which of said functional elements is a synchroniser to thereby identify if there is a synchronisation problem between for said at least one signal passing from one clock environment to another.

2. A method as claimed in claim 1, wherein in the simulation step, a plurality of simulations are carried out with one or more of the following clock signals in said one clock environment and said another clock environment:

a) the same clock frequency and phase in said clock environments;

b) the same clock frequency and different phase in said clock environments; and

c) different clock frequencies in the clock environments.

3. A method as claimed in claim 1, wherein in said simulation step, said one clock environment and said another clock environment have the same clock frequency and phase.

4. A method as claimed in claim 1, wherein in said simulation step, said one clock environment and said another clock environment have the same clock frequency and a first phase difference.

5. A method as claimed in claim 4, wherein said simulation step is repeated with said one clock environment and said other clock environment having the same clock frequency and a second phase difference.

6. A method as claimed in claim 5, wherein said second phase difference is of opposite polarity to said first phase difference.

7. A method as claimed in claim 1, wherein in said simulation step, said one clock environment and said another clock environment have a different clock frequency.

8. A method as claimed in claim 1, wherein said determining step comprises the step of tuning the predetermined time such that an unknown state propagates through only a part of said circuit.

9. A method as claimed in claim 1, wherein said determining step comprises using warnings identifying the functional element which is a source of the unknown state and determining if said source has a synchronising function in said circuit.

10. A method as claimed in claim 1, wherein the simulation and determining steps are repeated a plurality of times.

11. A method of claim 1, wherein said determination step is arranged to identify if a functional element which is a source of said unknown state propagation is a hazard or a synchroniser.

12. A method as claimed in claim 1, wherein in said determining step, wherein if a functional element is determined to be a synchroniser, said functional element is arranged such that the unknown state is not propagated.

13. A method as claimed in claim 1, wherein if first and second functional elements are identified as first and second synchronisers, said second synchroniser is arranged such that the unknown state is not propagated.

14. A method as claimed in claim 1, wherein a first element is identified as a synchroniser, comprising the step of determining the propagation of an unknown state for the remainder of the clock cycle by presence of different values before and after the unknown state presented at an input of the synchroniser.

15. A method as claimed in claim 1, wherein said circuit is represented at gate level.

16. A method as claimed in claim 1, wherein said circuit is designed in HDL.

17. A method as claimed in claim 1, wherein said method is carried out on a simulation tool.

18. A method as claimed in claim 1, wherein said timing event comprises a clock edge.

19. A method as claimed in claim 1, wherein said functional elements comprise logic gates.

20. A method as claimed in claim 19, wherein said logic gates comprise flip-flops.